

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 2

PATENT  
Filed: August 16, 2001

AI  
Cant

1. (original) A method for concealing errors in texture partition of a video packet, comprising:
  - determining a particular macroblock within the texture partition where error is detected;
  - concealing the error starting at the particular macroblock;
  - evaluating image smoothness of concealed macroblocks;
  - repeating said concealing and evaluating with one more macroblock added prior to the previous particular macroblock, said repeating done until all macroblocks in the texture partition have been concealed; and
  - selecting a set of macroblocks, including a combination of decoded and concealed macroblocks, that produces best image smoothness.
2. (original) The method of claim 1, further comprising:
  - storing all decoded macroblocks of texture data in the texture partition up to the particular macroblock.
3. (original) The method of claim 1, wherein said concealing the error starting at the particular macroblock includes performing motion compensated temporal replacements of macroblocks starting at the particular macroblock
4. (original) The method of claim 3, wherein said performing motion compensated temporal replacements is done for those macroblocks whose motion vectors have changed

1108-121.AMD

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 3

PATENT  
Filed: August 16, 2001

- a1*  
*Cont*
5. (original) The method of claim 1, wherein said evaluating image smoothness of concealed macroblocks includes computing smoothness of macroblock boundaries
6. (original) The method of claim 5, wherein said smoothness of macroblock boundaries is measured by summing pixel value mismatches between macroblock boundary pixels.
7. (original) The method of claim 6, wherein said summing pixel value mismatches includes storing partial mismatch values.
8. (original) The method of claim 6, wherein said summing pixel value mismatches includes summing squares of the pixel value differences.
9. (original) The method of claim 6, wherein said summing pixel value mismatches includes summing squares of the pixel value differences that weighs the pixel value mismatches between macroblocks belonging to different video packets differently.
10. (original) The method of claim 9, wherein the pixel value mismatches between macroblocks that belong to different video packets may be configured to weigh more than the pixel value mismatches between macroblocks that belong to same video packets.

116R-121.AMD

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 4

PATENT  
Filed: August 16, 2001

a!  
Cont

11. (original) The method of claim 6, wherein said pixel value mismatches are computed by reusing the partial mismatch values from previous iteration.

12. (original) The method of claim 1, further comprising:  
detecting the error in the video packet.

13. (original) The method of claim 12, wherein said detecting includes detecting invalid variable length code.

14. (original) The method of claim 12, wherein said detecting includes detecting inconsistent resynchronization header information.

15. (original) The method of claim 12, wherein said detecting includes detecting receipt of out-of-range motion vectors.

16. (currently amended) The method of claim 2, wherein said detecting includes DCT coefficient counts greater than a predetermined amount of approximately 64 pixels for a macroblock and Y/Cr/Cb pixel values out of range.

17. (original) The method of claim 2, wherein said selecting a set of macroblocks includes recovering some of the stored decoded macroblocks

1108-121.AMD

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 5

PATENT  
Filed: August 16, 2001

*a1*  
*cont*  
18. (original) The method of claim 17, wherein said some of the stored decoded macroblocks include decoded macroblocks up to a macroblock that produced the best image smoothness.

19. (original) A method for concealing errors in texture partition of a video packet, comprising:  
determining a particular location within the texture partition where error is detected;  
concealing the error in texture data starting at the particular location;  
evaluating image smoothness of the concealed texture data;  
repeating said concealing and evaluating with one more texture data unit added prior to the previous particular location, said repeating done until all texture data units in the texture partition have been concealed;  
and  
selecting a set of texture data units, including a combination of decoded and concealed texture data units, that produces best image smoothness.

20. (original) The method of claim 19, wherein said concealing the error in the texture data starting at the particular location includes performing motion compensated temporal replacements of texture data units starting at the particular location.

21. (original) An error concealment system for texture partition of a video packet, comprising:  
an error location detector to receive video packets, and determine a particular macroblock within the texture partition where error is detected;  
an error concealment element to conceal the error starting at the particular macroblock;

1168-121.AMD

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 6

PATENT  
Filed: August 16, 2001

an image smoothness evaluator to evaluate the concealed macroblocks;

a selector to select a set of macroblocks, including a combination of decoded and concealed macroblocks, that produces best image smoothness.

22. (original) The system of claim 21, wherein said error concealment element includes a motion compensated temporal replacement element.

23. (original) The system of claim 21, further comprising:

a storage element to store all decoded macroblocks of texture data in the texture partition up to the particular macroblock.

24. (original) A computer readable medium containing executable instructions which, when executed in a processing system, causes the system to conceal errors in texture partition of a video packet, comprising:

determining a particular macroblock within the texture partition where error is detected;

concealing the error starting at the particular macroblock;

evaluating image smoothness of concealed macroblocks;

repeating said concealing and evaluating with one more macroblock added prior to the previous particular macroblock, said repeating done until all macroblocks in the texture partition have been concealed; and

selecting a set of macroblocks, including a combination of decoded and concealed macroblocks, that produces best image smoothness.

1168-121.AMD

CASE NO.: 50R4781  
Serial No.: 09/932,127  
April 14, 2004  
Page 7

PATENT  
Filed: August 16, 2001

*a' level*  
25. (original) The computer medium of claim 24, further comprising:

storing all decoded macroblocks of texture data in the texture partition up to the particular macroblock.

11/08 121.AMD